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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,329	04/14/2004	Yeshwanth Narendar	1075-E4371	5396
34456	7590	08/24/2005	EXAMINER	
TOLER & LARSON & ABEL L.L.P. 5000 PLAZA ON THE LAKE STE 265 AUSTIN, TX 78746			MALDONADO, JULIO J	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

11A

Office Action Summary	Application No.	Applicant(s)	
	10/824,329	NARENDAR ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 June 2005.
 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-53 is/are pending in the application.
 4a) Of the above claim(s) 22-53 is/are withdrawn from consideration.
 5) ☐ Claim(s) _____ is/are allowed.
 6) ☒ Claim(s) 1-21 is/are rejected.
 7) ☐ Claim(s) _____ is/are objected to.
 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1075-E4371; 200502</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-21 in the reply filed on 06/16/2005 is acknowledged. The traversal is on the ground(s) that it does not create an undue burden and that the USPTO has historically examined applications containing multiple set of claims. This is not found persuasive because, as mentioned in the restriction mailed on 05/17/2005, there are two independent and distinct inventions (i.e., method claims and apparatus claims), and it would require a separate search, giving a serious burden on the examiner.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2 and 12-17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldstein et al. (U.S. 5,494,439).

In reference to claims 1 and 12-17, Goldstein et al. (Figs.1-3) teach a semiconductor processing component comprising an ultraclean SiC surface, wherein said outer surface portion of the component is free from metal impurities, wherein said surface is cleaner than an interior bulk of said semiconductor component, and wherein

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said metal impurities comprise aluminum, sodium and iron (column 2, line 47 – column 8, line 7).

Goldstein et al. also teach wherein metal impurity diffusing from the surface of said silicon carbide component is 60-90% less than the diffusion of said metals from the bulk of said component (column 7, lines 29 – 44). However, Goldstein et al., fail to teach wherein said outer surface impurity level is not greater than 100 times a bulk impurity level. However, the selection of the impurity level range is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species to obtain a desired surface, and furthermore, because Goldstein et al. is directed to a semiconductor component having reduced metal impurity levels on its surface. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use Goldstein et al. to arrive at the claimed invention.

In reference to claim 2, Goldstein substantially teach all aspects of the invention, but fail to disclose wherein the bulk impurity level is measured at a depth of at least 3μ , from an outer surface of the outer surface portion. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie

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obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In reference to claims 19 and 20, Goldstein et al. teach wherein said component may include boats, cantilevers, tubes, liners, pedestals and pins (column 3, lines 2 – 4).

4. Claims 3-11, 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldstein et al. (U.S. 5,494,439) as applied to claims 1, 2 and 12-17, 19 and 20 above, and further in view of Bosch (U.S. 6,890,861 B1).

In reference to claims 3-7, 10, 11, Goldstein et al. substantially teach wherein said SiC component are formed by a sintering process but fail to teach wherein said components are formed by a CVD process. However, Bosch teaches silicon carbide components or silicon carbide/silicon components such as liners, process tubes, paddles and boats, formed by either sintering and/or CVD processes (column 3, lines 32 – 38). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Goldstein et al. and Bosch to enable the components of Goldstein et al. to be formed according to the teachings of Bosch because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed components of Goldstein

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et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 8 and 9, the combined teachings of Goldstein et al. and Bosch substantially teach all aspects of the invention but fail to disclose wherein said CVD-SiC layer has a thickness within a range of about 10 to about 1,000 μm . Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In reference to claim 18, the combined teachings of Goldstein et al. and Bosch teach wherein conventional contaminants in SiC components include metals such as Fe and Cr (Bosch, column 1, lines 46 – 57). The combined teachings of Goldstein et al. and Bosch fail to teach wherein the bulk impurity level is not greater than 1×10^{17} atoms/ccFe and not greater than 1×10^{15} atoms/ccCr. However, the selection of the

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impurity level range is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species to obtain a desired surface, and furthermore, because Goldstein et al. and Bosch are directed to a semiconductor component having reduced metal impurity levels on its surface (Goldstein et al., column 2, lines 47 – 58 and Bosch, column 4, lines 15 – 20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use Goldstein et al. and Bosch to arrive at the claimed invention.

In reference to claim 21, the combined teachings of Goldstein et al. and Bosch teach wherein SiC components are conventionally machined prior to treatments to reduce surface impurity levels (Bosch, column 4, line 15 – column 6, line 50).

Conclusion

5. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (<http://portal.uspto.gov/external/portal/pair>) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.


6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at <http://www.uspto.gov/web/info/2800.htm>.

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Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
August 15, 2005


George Fourson
PRIMARY EXAMINER
2823